REMARKS

Claims 1-4 are all the claims pending in the application.

Formal matters

Applicant acknowledges that the Examiner has accepted the drawing filed on February 05, 2007. Applicant also notes that the Examiner acknowledges the claim to foreign priority and the receipt of the certified copy of the priority document. Furthermore, Applicant notes that the Examiner acknowledges considering the references submitted with the Information Disclosure Statements (IDS) filed on March 17, 2006 and February 05, 2004.

However, Applicant disagrees with the Examiner's characterization of the references submitted with the IDS as Applicant's admitted prior art. Applicant does not indicate admittance of the references submitted with IDS as prior art in the Specification or the IDS. In fact, page 2, lines 11-12 of the IDS filed on March 17, 2006 and page 2, lines 3-4 of the IDS filed on February 05, 2004 specifically state "the submission of the listed documents is not intended as an admission that any such document constitutes prior art against the claims of the present application."

Claims rejections

Claim 1 and 2 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yasuhiro (JP 07-170167) in view of Tenshiyuu (JP 10-173510). Applicant traverses the rejections at least for the following reasons.

Claim 1

Claim 1, *inter alia*, recites a first resistor having a resistance value with which a current flowing through the first resistor is smaller than an output current of said first potential level from said signal generating unit and a second resistor having a resistance value with which a current flowing through said second resistor is smaller than an output current from said signal generating unit having said second potential level.

In the rejection of claim 1 at page 3, line 15 of the Office Action, the Examiner admits that Yasuhiro does not disclose the above noted unique features as defined by claim 1. However, Examiner asserts that Tenshiyuu teaches the feature missing in Yasuhiro (page 3, lines 19-21 of the Office Action). Applicant respectfully disagrees.

Tenshiyuu is directed to a conversion circuit that converts an HSTL (High Speed Transceiver Logic) signal into PECL (Pseudo ECL; false emitter coupled logic). Tenshiyuu discloses a pull-up resistor 5 and a pull down resistor 6 (Figure 1). However, Tenshiyuu does not disclose a first resistor having a resistance value with which **a current flowing through the first resistor is smaller than an output current of said first potential level** from said signal generating unit and a second resistor having a resistance value with which **a current flowing through said second resistor is smaller than an output current** from said signal generating unit having **said second potential level**.

In particular, Tenshiyuu discloses that a capacitor part, which contains capacitor 4-1 and 4-2, converts an HSTL into an AC signal (Figure 1, paragraph [0007]). The AC signal is changed in to a PECL level signal by shifting reference potential level by the pull-up resistor and the pull down resistor (paragraph [0007]). Tenshiyuu discloses that the pull-up resistor 5 and

pull down resistor 6 are used to shift the reference potential level (paragraph 0011) and does not disclose pull-up resistor 5 (alleged first resistor) having a resistance value with which a current flowing through the pull-up resistor 5 is smaller than an output current of said first potential level from said signal generating unit and the pull-down resistor 6 (alleged second resistor) having a resistance value with which a current flowing through said pull-down resistor 6 (alleged second resistor) is smaller than an output current from said signal generating unit having said second potential level.

Furthermore, the Examiner asserts that it would have been obvious to modify the system of Yasuhiro based on the teachings of Tenshiyuu in order to provide stability (paragraph 20). Tenshiyuu discloses that stability is acquired by setting the capacity value to a certain optimal value (paragraph [0020]). However, Yasuhiro, which is directed to a level shifter for an AC signal for the purpose of eliminating self-exciting oscillation, discloses a DC-cut capacitor 1 that removes the DC component of the AC signal (paragraph [0007]). Applicant submits that since Yasuhiro already discloses a capacitor that removes DC component and possibly provide stability, it would not have been obvious to one of ordinary skill to modify the system of Yasuhiro based on the teaching of Tenshiyuu in order to provide stability since Yasuhiro already takes steps to provide stability.

In view of the above, Applicant respectfully submits that claim 1 is allowable and requests the Examiner to withdraw the rejection of claim 1.

Claim 2

Applicant respectfully submits that claim 2 depends from claim 1, and therefore, claim 2 is allowable at least by virtue of its dependency.

Claim 3

Applicant respectfully submits that since Orii does not cure the deficiency noted above with respect to claim 1 and since claim 3 depends from claim 1, claim 3 is allowable at least by virtue of its dependency.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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